Post Details	Last Updated:		
Faculty/Administrative/Service Department	Faculty of Engineering & Physical Sciences (FEPS) Institute for Communication Systems (ICS)		
Job Title	Research FPGA Developer		
Job Family	Technical and Experimental	**Job Level**	5
Responsible to	Wireless Systems Lab group leader		
Responsible for (Staff)	n/a		

Job Purpose Statement

To undertake a range of development and research activities in the field of physical layer signal processing for future mobile wireless communication systems, in accordance with the specified internal and external 6GIC/5GIC research projects.

The post holder will assume responsibility for specific areas of the specified internal and external 6GIC/5GIC research projects and will work as part of the Wireless Systems Lab group under the direction of the Wireless System Lab group leader.

Key Responsibilities

- To contribute to the specified internal and external 6GIC/5GIC research projects in collaboration with other members of the Wireless Systems Lab group or other members of 6GIC/5GIC.
- To undertake a range of development and research activities in the field of physical layer signal processing for future mobile wireless communication systems in accordance with the specified internal and external 6GIC/5GIC research projects.
- To design, develop and validate efficient algorithmic architectures for current and future mobile wireless communication systems, mainly targeting physical layer functionality on Field-Programmable Gate Arrays (FPGAs) and x86 general-purpose processors.
- To formally document new developments and where necessary provide training to external project partners and colleagues in order to fully exploit their potential.
- To liaise with other members of the Wireless Systems Lab group, providing specialist advice and guidance where needed to ensure effective transfer of skills/knowledge and compliance with regulations and code of practice.
- To plan and manage own development and research activities with minimal regular supervision.
- The post holder may occasionally be required to supervise more junior research/development staff.

All staff are expected to:

- Positively support equality of opportunity and equity of treatment to colleagues and students in accordance with the University of Surrey Equal Opportunities Policy.
- Work to achieve the aims of our Environmental Policy and promote awareness to colleagues and students.
- Follow University/departmental policies and working practices in ensuring that no breaches of information security result from their actions.
- Ensure they are aware of and abide by all relevant University Regulations and Policies relevant to the role.
- Undertake such other duties within the scope of the post as may be requested by your Manager.
- Work supportively with colleagues, operating in a collegiate manner at all times.

Help maintain a safe working environment by:

- Attending training in Health and Safety requirements as necessary, both on appointment and as changes in duties and techniques demand.
- Following local codes of safe working practices and the University of Surrey Health and Safety Policy.

Elements of the Role

Planning and Organising

- The post holder will be primarily a technical expert but will be required to demonstrate good self-project management skills within a very complex technical environment.
- The post holder will plan and organise their continuous technical hardware and software development to ensure alignment with evolving research and development requirements.
- The post holder will be responsible for delivering project plans for their own work and preparing appropriate information to ensure managers, strategic boards and external stakeholders are kept up to date with the relevant milestones of their project work.
- There will be involvement in various aspects of project life-cycle through initial analysis, development, commissioning, testing, documenting, deployment and finally hand-over to the administration team for on-going management and support.

Problem Solving and Decision Making

- The post holder is expected to operate with a high degree of autonomy within their defined project area, with minimum referral to the Wireless System Lab leader.
- The post holder is expected to undertake a range of development and research activities in a team-based environment operating in an agile manner to best use the people as well as hardware and software resources available at the 6GIC/5GIC.
- The ability to resolve internal resource and technical issues whilst maintaining positive external relationships is a key part of the role.
- The post holder is required to be a confident communicator as they need to gain the necessary information from project partners and researchers to progress the project and need to persuade individuals who they have no authority over to complete tasks to agreed deadlines and within project schedules.
- The post holder must be capable of making well-judged decisions on how best to allocate their available time to individual projects to best fit with changing strategic priorities.

Continuous Improvement.

- The post holder is expected to carry out the design work associated with the specified internal and external 6GIC/5GIC research projects to maintain quality of outputs to provide basis for the University to expand its activity with industry partners and other research institutions.

- Ensure that the designed elements are “future-proofed” to facilitate future development in line with the likely rapid evolution of mobile wireless communication technology.

Accountability

- The post holder will undertake FPGA and software development to deliver first class outputs to internal and external 6GIC/5GIC partners. The post holder will be expected to do this with minimal regular supervision. Typically the post holder will be expected to give formal monthly update summaries to the Wireless Systems Lab leader or Project Technical Manager.
- The post holder will be responsible for designing and developing specific aspects of the specified internal and external 6GIC/5GIC projects with minimal guidance from the Wireless Systems Lab leader or Project Technical Manager. This is an extremely technically demanding role and the post holder will be fully accountable for their technical decisions in this area.
- The post holder must display a professional approach and confident communication style as they represent a major part of the outward face of the University through the highly visible activities of the 6G/5G programme.

Dimensions of the role

- This post is a highly technical and currently unique in the world, which will by definition have to evolve as the project work progresses.
- This post has no staff responsibility.
- This post has no budgetary responsibility.

Supplementary Information

Recent government reports on the HE sector, such as the influential Witty review, have placed emphasis on UK universities acting as “engines of the economy”. Both BIS and HEFCE are developing new funding streams which will increasingly favour high quality research programmes with the capacity for significant economic impact and the 6GIC/5GIC is considered as an exemplar in this regard.

Person Specification This section describes the sum total of knowledge, experience & competence required by the post holder that is necessary for standard acceptable performance in carrying out this role.

Qualifications and Professional Memberships		
Degree level qualification in Electronics or Computing or substantial vocational experience within the field.		E
Project management qualification or equivalent relevant experience.		D
Technical Competencies (Experience and Knowledge) This section contains the level of competency required to carry out the role (please refer to the Competency Framework for clarification where needed and the Job Matching Guidance).	**Essential/ Desirable**	**Level 1-3**
Design and development of algorithms targeting high throughput and low-latency on Xilinx FPGAs using RTL.	E	3
Recent experience in the development of physical layer digital signal processing algorithms (e.g., forward error codrrection).	E	3
Good understanding of signal processing for wireless communication systems.	E	2
Experience in development on Linux operating systems	E	2
An overall working knowledge of cellular networks (e.g.,: LTE, 5GNR).	E	2
Experience with a high-speed FPGA protocol, e.g., PCIe or 10GE.	D	n/a

Experience with HLS design methodologies (e.g., using Xilinx System Generator for DSP)	D	n/a
Experience in high-performance programming targeting signal processing algorithms for high throughput and low-latency using C/C++ on x86 architectures	D	n/a
Experience in programming on nVIDIA GPUs using the CUDA API.	D	n/a
Prior experience with wireless research platforms (e.g., Open Air Interface with USRPs).	D	n/a

Special Requirements:	**Essential/ Desirable**
Must be prepared to travel throughout the UK and internationally	D
Able to drive and has own car	D
Core Competencies This section contains the level of competency required to carry out this role. (Please refer to the competency framework for clarification where needed). n/a (not applicable) should be placed, where the competency is not a requirement of the grade.	**Level 1-3**
Communication	3
Adaptability / Flexibility	3
Customer/Client service and support	1
Planning and Organising	3
Continuous Improvement	3
Problem Solving and Decision Making Skills	3
Managing and Developing Performance	3
Creative and Analytical Thinking	3
Influencing, Persuasion and Negotiation Skills	2
Strategic Thinking & Leadership	2

This Job Purpose reflects the core activities of the post. As the Department/Faculty and the post holder develop, there will inevitably be some changes to the duties for which the post is responsible, and possibly to the emphasis of the post itself. The University expects that the post holder will recognise this and will adopt a flexible approach to work. This could include undertaking relevant training where necessary.
Should significant changes to the Job Purpose become necessary, the post holder will be consulted and the changes reflected in a revised Job Purpose.

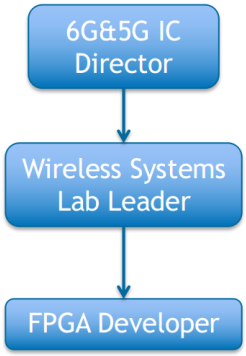
Organisational/Departmental Information & Key Relationships

Background Information

ICS is the largest academic research institute in Europe specialising in all aspects of ICT (Information and Communication Technologies). It is home to over 200 researchers with expertise in all communication and broadcasting systems and has developed the best in class large scale testbeds for research and innovation and enjoys the state-of-the-art lab and computing facilities.

Established in 2012, 5GIC is the world's first dedicated centre in researching end-to-end aspects of 5G and works closely with national and international leading academic institutes and key industrial partners. In November 2020, 6GIC was officially launched with parallel research undertaken in both 5G+ and 6G for 2030+.

Department Structure Chart



Relationships:

Internal

The post holder will liaise primarily with the Wireless System Lab leader and Wireless Systems Lab team, as well as other staff within the ICS. There will also be a requirement to liaise with support and technical staff within the Faculty of Engineering and Physical Sciences.

External

Development and integration of the hardware and software components will require very significant technical and project management skills as well as dealing directly with 5G Industry partners when required.