Post Details	Last Updated: 06.12.2024		
Faculty/Administrative/Service Department	Faculty of Engineering and Physical Sciences		
Job Title	Field Programmable Gate Array Technician		
Job Family	Technical and Experimental	**Job Level**	3
Responsible to	Dr Chris Bridges, ARIA Photonics PI		
Responsible for (Staff)	N/A		

Job Purpose Statement *This should be an accurate, concise, un-detailed statement (short paragraph) of what the post is and why the post exists in terms of its contribution or result e.g. improved student/staff experience, increasing University funds etc*.

To provide FPGA and VHDL programming and technician support to the laser payload being developed under the ARIA Photonics Project in Surrey Space Centre.

ARIA Photonics aims to develop critical signal processing avionics and robust all-fibre architecture for space-based laser systems to enable a new, innovative generation of smaller, lighter, more resilient portable isotopologue and ppb sensing to deliver a step change in both performance and cost.

This relies on adapting telecoms industry COTS components and software radio FPGA/DSP techniques towards a new all-fibre space-qualified stabilised laser systems for geodesy with equivalent performance to laboratory systems. A flexible digital control system will enable automated operation in harsh environments, with full testing in simulated space environments undertaken.

Key Responsibilities This document is not designed to be a list of all tasks undertaken but an outline record of the main responsibilities (5 to 8 maximum)

1. To write simulation files for the current VHDL control and filter codes to make performance analysis.
2. To recommend any restructuring of the ARIA Photonics firmware.
3. To provide updated FDIR and risk analysis updates using Xilinx critical bits methodology.
4. To support the hardware and software implementation of new ADC and DAC filters and configurations
5. To create digital test result logs that details the ARIA Photonics payload performance.
6. To provide general support towards the ARIA Photonics project document delivery.

N.B. The above list is not exhaustive.

All staff are expected to:

- Positively support equality of opportunity and equity of treatment to colleagues and students in accordance with the University of Surrey Equal Opportunities Policy.
- Work to achieve the aims of our Environmental Policy and promote awareness to colleagues and students.
- Follow University/departmental policies and working practices in ensuring that no breaches of information security result from their actions.
- Ensure they are aware of and abide by all relevant University Regulations and Policies relevant to the role.
- Undertake such other duties within the scope of the post as may be requested by your Manager.
- Work supportively with colleagues, operating in a collegiate manner at all times.

Help maintain a safe working environment by:

- Attending training in Health and Safety requirements as necessary, both on appointment and as changes in duties and techniques demand.
- Following local codes of safe working practices and the University of Surrey Health and Safety Policy.

Elements of the Role

This section outlines some of the key elements of the role, which allow this role to be evaluated within the University's structure. It provides an overview of what is expected from the post holder in the day-to-day operation of the role.

Planning and Organising

- The post holder will organise and prioritise their work to ensure all parts of the ARIA Photonics activities are ready to meet the ARIA Photonics project targets.
- The post will receive guidance and support from the ARIA Photonics Project PI and team where appropriate.

Problem Solving and Decision Making.

- The post holder is expected to independently apply their technical and practical knowledge of existing laser systems to ensure that the ARIA Photonics Project advances.
- The post holder is required to recognise that when problems/issues arise to contact a senior member of the ARIA Photonics Project team for guidance.

Continuous Improvement

- The post holder is expected to understand the latest FPGA/VHDL tools and ensure the ARIA Photonics project moves towards state of the art systems.
- The post holder is expected to take a pro-active approach to their work methods.

Accountability

- The post holder is expected to ensure compliance with lab safety standards for all staff, students and visitors in the immediate vicinity of the ARIA Photonics payload working within the Surrey Space Centre.
- The post holder will work with limited supervision and the may report progress as required by the ARIA Photonics PI.
- The post holder is expected to take all necessary action to ensure the ARIA Photonics payload meets system requirements.

Dimensions of the role

- The post holder will be working on hardware and software development with Surrey Space Centre staff and students.
- The post holder may also be interfacing with external contractors.

Person Specification This section describes the sum total of knowledge, experience & competence required by the post holder that is necessary for standard acceptable performance in carrying out this role.

Qualifications and Professional Memberships	
HNC, A level, NVQ 3 or equivalent standard in the relevant specialist area, plus a number of years' relevant work experience OR Broad practical work experience in a relevant technical or scientific role	E

Technical Competencies (Experience and Knowledge) This section contains the level of competency required to carry out the role (please refer to the Competency Framework for clarification where needed and the Job Matching Guidance).	**Essential / Desirable**	**Level 1-3**
Knowledge and experience in FPGA hardware development	E	3
Knowledge and experience in VHDL software simulation	E	3
Experience in integrating laser and ADC / DAC digital systems	D	N/A

Core Competencies This section contains the level of competency required to carry out this role. (Please refer to the competency framework for clarification where needed). n/a (not applicable) should be placed, where the competency is not a requirement of the grade.	**Level 1-3**
Communication	3
Adaptability / Flexibility	3
Customer/Client service and support	2

Planning and Organising	2
Continuous Improvement	2
Problem Solving and Decision Making Skills	2
Managing and Developing Performance	N/A
Creative and Analytical Thinking	2
Influencing, Persuasion and Negotiation Skills	2
Strategic Thinking & Leadership	N/A

This Job Purpose reflects the core activities of the post. As the Department/Faculty and the post holder develop, there will inevitably be some changes to the duties for which the post is responsible, and possibly to the emphasis of the post itself. The University expects that the post holder will recognise this and will adopt a flexible approach to work. This could include undertaking relevant training where necessary.

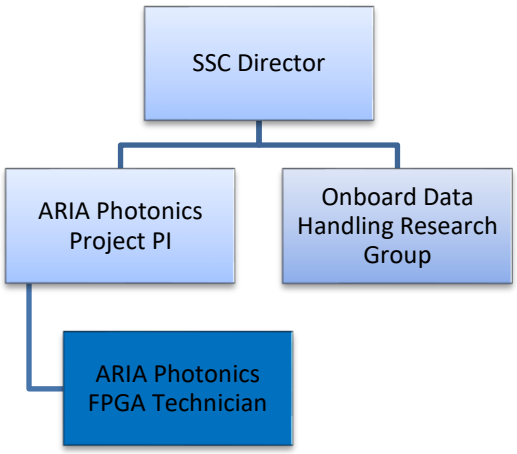
Should significant changes to the Job Purpose become necessary, the post holder will be consulted and the changes reflected in a revised Job Purpose.

Organisational/Departmental Information & Key Relationships

Background Information

The Surrey Space Centre (SSC) at the University of Surrey is a world leading Centre of Excellence in Space Engineering. The On-board Data Handling Group leads the expertise if hardware and software in advanced computing payloads.

Department Structure Chart



Relationships

Internal

- The post holder is required to develop relationships within Surrey Space Centre's academic and non-academic staff using the labs.
- The post holder is expected to communicate with other FEPS depts. as appropriate to meet Health and Safety obligations

External

- The post holder may be expected to communicate with contractors and suppliers.